ABSTRACT

An output buffer circuit comprises an input terminal, an output terminal first and second inverters, a pull up control circuit, a pull down control circuit and first and second output transistors. Each of the first and second inverters is connected to the input terminal for outputting a signal having a slow rise up and fall down characteristic. Both of the pull up and pull down control circuits are connected to the input terminal and the output terminal. The pull up control circuit pulls up an output voltage of the first inverter when the output signal of the first inverter has a level lower than a first threshold voltage level. The pull up control circuit stops the pull up operation when the level of the output signal of the first inverter exceeds the first threshold voltage level. The pull down control circuit pulls down an output voltage of the second inverter when the output signal of the second inverter has a level higher than a second threshold voltage level. The pull down control circuit stops the pull down operation when the pull down control circuit becomes lower than the second threshold voltage level. The first output transistor has a source connected to a first power source, a drain connected to the output terminal and a gate connected to the first inverter. The second output transistor has a source connected to a second power source, a drain connected to the output terminal and a gate connected to the second inverter.